Amendments to the Claims

1-17. Cancelled.

18. (New) A bus interface and power control system, comprising:

a connection for a primary power supply (20);

a transceiver (34) providing a data interface to a single node (12) on a data communication bus (10) and able to provide a bus-activity signal (94) when data activity is monitored on the data communication bus (10) during a low power mode supported by the primary power supply (20);

a protocol controller (42) for decoding data messages passed through the transceiver (34) from said data communication bus (10), and for providing a gate signal (54) when a decoded message matches a particular pattern in storage;

a first voltage regulator (32) for supplying additional power (92) to the transceiver (34) and for supplying operating power (62) to the protocol controller (42), both in a medium power mode engaged when said bus-activity signal (94) is received;

a second voltage regulator (34) for supplying operating power (82) in a high power mode to an applications processor (44) when said gate signal (54) is received;

wherein, the first and second voltage controllers (32 and 34) are off during said low power mode, the first voltage controller (32) is on during said medium power mode, and both the first and second voltage controllers (32 and 34) are on during said high power mode; and

and wherein, said low power mode of operation is returned to automatically.

19. (New) The interface and power control system of Claim 18, wherein:

the second voltage regulator (34) further provides a reset signal (84) to said applications processor (44).

20. (New) The interface and power control system of Claim 18, further comprising:

a plurality of addressable nodes (12) on bus (10) with corresponding application processors (44) are provided such that pre-selected messages communicated on bus (10) can power-up and power-down respective applications processors (44) and thereby conserve overall operating power taken from the primary power supply (20).

21. (New) A method of conserving operating power in a bus-oriented system (100) with many applications processors (44), comprising:

providing constant power from a primary power supply (20) to a plurality of bus transceivers (34) each connected to a respective node (12) on a bus (10);

monitoring said bus (10) for data activity and if such activity is detected (94) then, enabling (92) a higher power mode of operation for said bus transceivers (34) and powering up a data decoder (42);

decoding said data activity with said data decoder (42) and providing a gate signal (54) if a particular message from storage is recognized;

powering up (82) a corresponding applications processor (44) as long as its associated gate signal (54) is being received;

wherein, each particular applications processor (44) is powered up for so long as there is data activity and particular messages on said bus (10) are recognized, wherein overall operating power taken from the primary power supply (20) is conserved by operating said data decoder (42) in a medium power mode when data activity is detected, and then only operating each applications processor (44) when they have been addressed and selected to operate as determined by the corresponding data decoder (42).